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~~METHOD FOR~~ STANDBY CIRCUITING OF ASSEMBLIES IN 1:N ~~REDUNDANCY~~

~~The invention is directed to a method according to the preamble of patent claim 1~~

~~Dependent on the demanded~~ failure dependability ~~of a~~ communication means, different redundancy structures can be provided for the associated peripheral line assemblies ~~pertaining thereto~~. Examples of this are the "1+1" or the "1:N" line assembly redundancy ~~as~~ described in "IEEE Journal on Selected Areas in Communications", Vol. 15, No. 5, June 1997, pages 795 through 806. For ~~Given~~ a "1+1" redundancy structure, two line assemblies are operated parallel in order to redundantly transmit message signal streams over them ~~thereover~~. However, only one of these redundant message signal streams is considered for the further-processing.

For ~~Given~~ a "1:N" line assembly redundancy, a single standby line assembly or standby circuit assembly is provided in addition to a plurality N of line assemblies. When a fault occurs ~~Given occurrence of a fault~~ on one of the N line assemblies, the standby line assembly is then used in its place ~~instead~~.

In the Prior Art, the standby circuiting of assemblies in 1:N redundancy requires a means that maintains all information about current conditions and events within a redundancy group. This means is thus in the position to decide about required standby circuiting measures. This high-ranking means is usually the maintenance-oriented higher-ranking means of the periphery assemblies. This means must also be in the position to implement necessary alternate routings in the shortest possible time (< 1 s) or, respectively, to control and monitor malfunction-free switchbacks so that the down time or, respectively, the data loss of the affected lines is minimized. The failure of a peripheral line assembly is recognized by the respectively neighboring peripheral assembly in this Prior Art.

Figure 2 illustrates ~~To facilitate understanding, let~~ the configuration employed in the Prior Art which uses a 1:N line assembly redundancy ~~be shown in~~ ~~Figure 2. A "1:N" line assembly redundancy is employed in accord~~

~~therewith~~. By way of example, only the peripheral line assemblies BG_1, BG_2 are shown, these being respectively allocated to one another in pairs. Both assemblies comprise connections V_1 to one another via which a mutual monitoring is implemented. Further, internal and external interfaces are allocated to the peripheral line assemblies $BG_1 \ldots BG_n$. The internal interfaces serve as interfaces to the assemblies AMX of the ATM switching network, whereas the external interfaces represent interfaces to the ~~trunks~~ connected trunks ~~hereto~~ for the other switching network devices. The assemblies $BG_1 \ldots BG_n$ also comprise connections V_2 to the assemblies AMX of the ATM switching network, ~~whereby~~; only the connection V_2 of the assemblies BG_1 to the assemblies AMX is shown here. All assemblies $BG_1 \ldots BG_n$ as well as the allocated internal and external interfaces are monitored and controlled by a higher-ranking ~~means~~ mechanism MPSA.

Let it then be assumed below that one of the peripheral line assemblies fails, for example BG_1. A corresponding message M_A is consequently delivered to the higher-ranking maintenance means MPSA. This then starts a diagnosis in order to localize the fault and, potentially, verify it.

In a first step, an attempt is made to directly address the down device BG_1. In the case assumed here that the affected peripheral assembly BG_1 has a total failure, this failure is not recognized by the higher-ranking mechanism ~~means~~ MPSA until after the expiration of a number of monitoring events. Only then can it be reliably assumed that assembly ~~he means~~ BG_1 can no longer be addressed and, thus, is no longer available. A diagnosis of the appertaining peripheral assembly is subsequently initiated for verification of the fault. The appertaining peripheral assembly is not configured until the ~~front~~-end ~~[sic]~~ of this diagnosis, the actual alternate routing being implemented only then. To this end, the internal and external interfaces must also be switched and the standby circuit assembly must be correspondingly activated.

This ~~In detail, this means~~ that the higher-ranking mechanism ~~means~~ MPSA sends a message to the standby circuit assembly, controls the switching of the external and

internal interfaces to the standby circuit assembly BG_E and sends information to the affected applications.

However ~~Therewith, however~~, the higher-ranking mechanism ~~means~~ MPSA is mainly occupied with standby circuiting measures, which results in a loss of system dynamics ~~dynamics of the system~~. Further, a number of other assemblies that actually do not participate in the switchover process itself are integrated in the switchover process~~. More~~ losing more valuable time ~~is thereby lost~~. Ultimately, such a configuration runs counter to the principle of decentrally arranged maintenance ~~wherein~~ in which the alternate routing is a job of the peripheral devices themselves.

Summary of the invention

The invention is based on the object of ~~disclosing a way of how~~ providing a way of implementing standby circuitings for peripheral assemblies ~~can be implemented~~ faster and more efficiently without restricting the system dynamics ~~dynamics of the system~~.

a2 ~~Proceeding from the features recited in the preamble of patent claim 1, this object is achieved by the features recited in the characterizing part thereof.~~

What is advantageous about the invention is, in particular, that the standby circuiting or, respectively, switchback of a malfunctioning assembly is undertaken by the peripheral assemblies themselves under the control of the standby circuit assembly, independently of a higher-ranking mechanism ~~means~~. The basic principles of 1+1 assembly redundancy are applied in this approach ~~thereby applied~~. The basic executive sequences of the 1+1 assembly redundancy are thereby largely transferred to the 1:N redundancy. This has the advantage that synergies can be employed and performance features that are already available for the 1+1 redundancy can also be made ~~rendered~~ usable for the 1:N redundancy. An example of this is the soft switching between individual peripheral assemblies and the standby circuit assembly in both directions without call interruption ~~with~~ and saving ~~salvaging of~~ charge data. The inventive step is comprised in ~~therein~~ that the principles of decentralized maintenance are consistently converted for the 1:N redundancy with the assistance of the standby circuit assembly, the switchover times are considerably improved and the quality of the redundancy is improved.

a3 ~~Advantageous developments of the invention are recited in the subclaims.~~

Brief Description of the Drawings

The invention is explained in greater detail below in the drawings and associated text on the basis of an exemplary embodiment.

~~Shown are:~~

Figure 1 is a pictorial schematic showing a configuration on which the inventive method is run;

Figure 2 is a pictorial schematic showing the conditions in the Prior Art.

Description of the Preferred Embodiments

Figure 1 shows a configuration on which the inventive method is run~~. In accord therewith,~~ in which peripheral line assemblies $BG_1 \ldots BG_n$ are provided, ~~whereby~~ only two of these peripheral line assemblies BG_1, BG_2 are shown. The two assemblies are respectively allocated to one another in pairs and comprise connections V_1 to one another via which a mutual monitoring is carried out. Further, internal and external interfaces are allocated to the peripheral line assemblies $BG_1 \ldots BG_n$. The internal interfaces serve as interfaces to the assemblies AMX of the ATM switching network, whereas the external interfaces represent interfaces to the ~~trunks~~ connected trunks hereto for the other switching network devices. The assemblies $BG_1 \ldots BG_2$ also comprise connections V_2 to the assemblies AMX of the ATM switching network, ~~whereby~~ only the connection V_2 of the assemblies BG_1 to the assemblies AMX is shown here. All assemblies $BG_1 \ldots BG_n$ as well as the allocated internal and external interfaces are monitored and controlled by a higher-ranking mechanism ~~means~~ MPSA. Further, a standby circuit assembly BG_E is provided in this 1:N redundancy group~~, this being~~ which is intended to take the place of the down assembly for an assembly outage ~~given the outage of an assembly~~. Ultimately, switches LPS and SB are provided that reroute the ATM cell streams between the internal or~~, respectively,~~ external interfaces and the peripheral line assemblies.

A pre-condition of the inventive method is that connections between the standby circuit assembly BG_E and all peripheral line assemblies are provided, so that a constant communication relationship~~s~~ [sic] prevails. Likewise, the standby circuit assembly BG_E must be in the position to switch the internal interfaces from a peripheral assembly to the standby circuit assembly. Further, the standby circuit assembly must be in the position of switching the external interfaces of a peripheral line assembly ~~assemblies [sic]~~ to the standby circuit assembly BG_E. Ultimately, every

peripheral line assembly must recognize the failure of its neighboring peripheral line assembly in order to be able to report a corresponding message to the standby circuit assembly BG_E.

~~It is assumed below that one of the peripheral line assemblies fails. Let this be the~~ If assembly BG_1 fails, the ~~The~~ failure is identified via the trunk V_1 by the paired, allocated assembly BG_2. Subsequently, the assembly BG_2 transmits a corresponding message M_E to the standby circuit assembly BG_E. Further, the higher-ranking means MPSA is likewise informed of the failure via a message M_A, so that a current image of the system configuration continues to be stored in the latter.

The failure of the peripheral line assembly BG_1 is also recognized by the assembly AMX that, as part of the switching network, comprises a connection V_2 to the down peripheral line assembly BG_1. The higher-ranking means MPSA is informed of the failure via a message M_{LPS}.

In response to the message M_E, the standby circuit assembly BG_E implements the alternate routing. First, the internal interfaces are switched. This ensues by driving a switch LPS that accomplishes a switching event S_1. Subsequently, the switchover of the external interfaces ensues by driving a switch SB that effects a switching event S_2. Only then is the standby circuit assembly BG_E activated, this now having the function of the down assembly BG_1 and handling the ATM message cell stream routed ~~thereover~~ over it before the failure.

The error handling on the higher-ranking ~~means~~ mechanism MPSA runs completely independently ~~thereof~~ of this process. The separation between the standby circuit that is controlled by the standby circuit assembly and the outage handling by the higher-ranking maintenance assembly becomes clear with reference to the present exemplary embodiment for the standby circuiting of a peripheral line assembly in 1:N redundancy.